WHAT IS CLAIMED IS:

1. A method of data transmission, said method comprising:

receiving a plurality of sets of input signals, each input signal having a series of state transitions synchronized to a data clock signal having a period T_CLK; and

transmitting a corresponding plurality of sets of output signals such that each output signal (1) corresponds to an input signal of the corresponding set, (2) passes along a corresponding one of a plurality of conductive paths, and (3) has a series of state transitions corresponding to the series of state transitions of the corresponding input signal,

wherein a time between a state transition on an input signal of one set and the corresponding state transition on the corresponding output signal exceeds a time between a state transition on an input signal of another set and the corresponding state transition on the corresponding output signal by a delay period T_DLY, and

wherein the period T_CLK is greater than the delay period T_DLY, and

wherein adjacent conductive paths that each carry an output signal of one set are separated by at least one conductive path that carries an output signal of another set.

2. The method of data transmission according to claim 1, wherein the delay period T_DLY is at least twice as long as a rise time of the data clock signal.

3. The method of data transmission according to claim 1, wherein each state transition of an output signal corresponds to a different one among the state transitions of the corresponding input signal.

4. The method of data transmission according to claim 1, wherein the plurality of conductive paths is fabricated on a semiconductor substrate, and

wherein said receiving and said transmitting occur on the semiconductor substrate.

5. The method of data transmission according to claim 4, wherein a length of each of the plurality of conductive paths is at least five centimeters.

6. The method of data transmission according to claim 1, wherein a distance between adjacent ones of the plurality of conductive paths is less than one hundred microns.

7. The method of data transmission according to claim 1, wherein a width of each of the plurality of conductive paths is less than one hundred microns.

8. The method of data transmission according to claim 1, wherein each one among the plurality of conductive paths includes a corresponding one of a plurality of parallel transmission lines, and

wherein said method further comprises coupling the data clock signal to one of the plurality of transmission lines.

9. The method of data transmission according to claim 1, wherein each one among the plurality of conductive paths includes a corresponding one of a plurality of buffers.

10. The method of data transmission according to claim 1, wherein transmitting each output signal among a first one of the plurality of sets of output signals includes latching the series of state transitions of the corresponding input signal onto the output signal in response to a first clock signal, and

wherein transmitting each output signal among a second one of the plurality of sets of output signals includes latching the series of state transitions of the corresponding input signal onto the output signal in response to a second clock signal.

11. The method of data transmission according to claim 10, wherein the first and second clock signals are based on the data clock signal, and

wherein a time between a state transition on the data clock signal and a corresponding state transition on the second clock signal exceeds a time between a state transition on the data clock signal and a corresponding state transition on the first clock signal by the delay period T_DLY.

12. A data transmitter configured and arranged to receive a plurality of input signals and to transmit a plurality of first output signals and a plurality of second output signals, each of the first and second output signals corresponding to a different one of the input signals and each being transmitted along a corresponding one of a plurality of conductive paths, said data transmitter comprising:

a plurality of first latches, each having (1) a clock input configured and arranged to receive a first clock signal including a series of first transitions, with consecutive first transitions being separated by a time period T_CLK, (2) a latch input configured and arranged to receive a corresponding one of the input signals, and (3) an latch output configured and arranged to produce a corresponding latch signal, each first latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each first transition; and

a plurality of second latches, each having (1) a clock input configured and arranged to receive a second clock signal based on the first clock signal and including a series of second transitions, with consecutive second transitions being separated by a time period T_CLK, (2) a latch input configured and arranged to receive a corresponding input signal, and (3) a latch output configured and arranged to produce a corresponding latch signal, each second latch being further configured and arranged to latch a data value from the corresponding input signal to the corresponding latch signal upon each second transition;

wherein each first output signal is based on a latch signal of a different one of the first latches and each second output signal is based on a latch signal of a different one of the second latches, and

wherein a time between a transition on an input signal and a corresponding transition on a corresponding second output signal exceeds a

time between a transition on an input signal and a corresponding transition on a corresponding first output signal by a delay period T_DLY, and

wherein the time period T_CLK is greater than the delay period T_DLY, and

wherein adjacent conductive paths that each carry one of the plurality of first output signals are separated by a conductive path that carries one of the plurality of second output signals.

13. The data transmitter according to claim 12, wherein the data transmitter and the plurality of conductive paths are fabricated on the same semiconductor substrate.

14. The data transmitter according to claim 12, wherein the data transmitter is further configured and arranged to receive an operating voltage from two power rails, and

wherein the two power rails are parallel to and on opposite sides of the plurality of conductive paths.

15. The data transmitter according to claim 12, wherein each one among the plurality of conductive paths includes a corresponding one of a plurality of parallel transmission lines, and

wherein the data transmitter is further configured and arranged to couple the first clock signal to one of the plurality of parallel transmission lines.

16. The data transmitter according to claim 12, said data transmitter further comprising a plurality of buffers, each buffer being coupled to a different one of the latch outputs of the first and second latches.

17. The data transmitter according to claim 12, said data transmitter further comprising a delay element configured and arranged to receive the first clock signal and to produce the second clock signal,

wherein the second clock signal is delayed with respect to the first clock signal by the delay period T_DLY.

18. The data transmitter according to claim 12, said data transmitter further comprising a plurality of delay elements, each configured and arranged to receive a different one of the second latch signals and to produce the corresponding second output signal.

19. The data transmitter according to claim 18, wherein the second clock signal is substantially identical to the first clock signal.

20. The data transmitter according to claim 12, wherein the delay period T_DLY is at least twice as long as a rise time of the data clock signal.

21. A system for data transmission, said system including:

a plurality of conductive paths; and

a data transmitter configured and arranged to receive a plurality of input signals, each having a series of state transitions synchronized to a data clock signal having a period T_CLK, and to transmit a plurality of first output signals and a plurality of second output signals,

wherein each of the first and second output signals corresponds to a different one of the input signals and has a series of state transitions corresponding to the series of state transitions of the corresponding input signal, and

wherein the data transmitter is further configured and arranged to transmit each of the first and second output signals along a corresponding one of the plurality of conductive paths, and

wherein a time between a state transition on an input signal and a corresponding state transition on a corresponding second output signal exceeds a time between a state transition on an input signal and a corresponding state transition on a corresponding first output signal by a delay period T_DLY, and

wherein the time period T_CLK is greater than the delay period T_DLY, and

wherein adjacent conductive paths that each carry one of the plurality of first output signals are separated by a conductive path that carries one of the plurality of second output signals.

22. The system for data transmission according to claim 21, wherein each state transition of an output signal corresponds to a different one among the state transitions of the corresponding input signal.

23. The system for data transmission according to claim 21, wherein the data transmitter and the plurality of conductive paths are fabricated on the same semiconductor substrate.

24. The system for data transmission according to claim 23, wherein a length of each of the plurality of conductive paths is at least five centimeters.

25. The system for data transmission according to claim 21, wherein a distance between adjacent ones of the plurality of conductive paths is less than one hundred microns.

26. The system for data transmission according to claim 21, wherein a width of each of the plurality of conductive paths is less than one hundred microns.

27. The system for data transmission according to claim 21, wherein the data transmitter is further configured and arranged to receive an operating voltage from two power rails, and

wherein the two power rails are parallel to and on opposite sides of the plurality of conductive paths.

28. The system for data transmission according to claim 21, wherein each one among the plurality of conductive paths includes a corresponding one of a plurality of parallel transmission lines, and

wherein the data transmitter is further configured and arranged to couple a clock signal based on the data clock signal to one of the plurality of parallel transmission lines.

29. The system for data transmission according to claim 21, wherein each among the plurality of conductive paths includes a corresponding one of a plurality of buffers.

30. The system for data transmission according to claim 21, wherein the delay period T_DLY is at least twice as long as a rise time of the data clock signal.

31. The system for data transmission according to claim 21, wherein the transmitter is configured and arranged to latch the series of state transitions of an input signal onto the corresponding one of the plurality of first output signals in response to a first clock signal, and

wherein the transmitter is configured and arranged to latch the series of state transitions of an input signal onto the corresponding one of the plurality of second output signals in response to a second clock signal.

32. The system for data transmission according to claim 31, wherein the first and second clock signals are based on the data clock signal.

33. The system for data transmission according to claim 21, said system further comprising a data receiver configured and arranged to receive

the plurality of first output signals and the plurality of second output signals and to produce a plurality of received signals,

wherein the data transmitter, the plurality of conductive paths, and the data receiver are fabricated on the same semiconductor substrate.

34. The system for data transmission according to claim 21, said system further comprising a data receiver configured and arranged to receive the plurality of first output signals and the plurality of second output signals and to produce a plurality of first received signals and a plurality of second received signals,

wherein each among the plurality of first received signals corresponds to one among the plurality of first output signals, and each among the plurality of second received signals corresponds to one among the plurality of second output signals, and

wherein each of the first and second received signals has a series of state transitions corresponding to the series of state transitions of the corresponding output signal, and

wherein the state transitions of each of the first and second received signals are synchronized to a received data clock signal, and

wherein one among the rising and falling edges of the data clock signal is synchronous with the other among the rising and falling edges of the received data clock signal.